CLAIMS

1. A programmable logic device comprising:

one or more horizontal routing channels;

one or more vertical routing channels;

one or more logic elements each configured to connect between one of said horizontal routing channels and one of said vertical routing channels, wherein said logic element comprises a logic block array and a memory block.

2. The programmable logic device according to claim 1, wherein said memory block is connected to one of said horizontal and one of said vertical routing channels.

3. The programmable logic device according to claim 2, wherein said memory block is configured as a synchronous dual port memory.

4. The programmable logic device according to claim 2, wherein said memory block is configured as an asynchronous dual port memory.

5. The programmable logic device according to claim 2, wherein said memory block is configured as a synchronous FIFO memory.

6. The programmable logic device of claim 1, wherein said memory block is placed within said logic block array.

7. The programmable logic device of claim 1, further comprising a plurality of I/O blocks, wherein each I/O block of said plurality of I/O blocks is connected to a different end of said horizontal and said vertical routing channels.

8. The programmable logic device of claim 7, wherein said I/O blocks are grouped into I/O banks.

9. The programmable logic device of claim 7, wherein said I/O blocks comprise configurable I/O cells.

10. The programmable logic device of claim 1, further comprising one or more dedicated inputs for I/O cell control.

11. The programmable logic device of claim 1, further comprising one or more dedicated clock inputs.

12. The programmable logic device of claim 11, further comprising a phase lock loop circuit configured to generate one or more global clock signals in response to one or more input clock signals.

13. The programmable logic device of claim 10, wherein said dedicated inputs for I/O control comprise a reset input.

14. The programmable logic device of claim 10, wherein said dedicated inputs for I/O control comprise an output enable input.

15. The programmable logic device of claim 10, wherein said dedicated inputs for I/O control comprise a clock enable input.

16. The programmable logic device of claim 11, further comprising a phase lock loop circuit configured to generate one or

more global clock signals by multiplying or dividing a frequency of a clock signal presented to said one or more dedicated clock inputs.